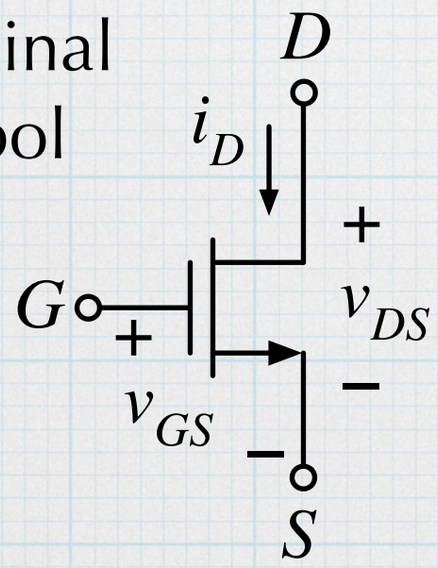
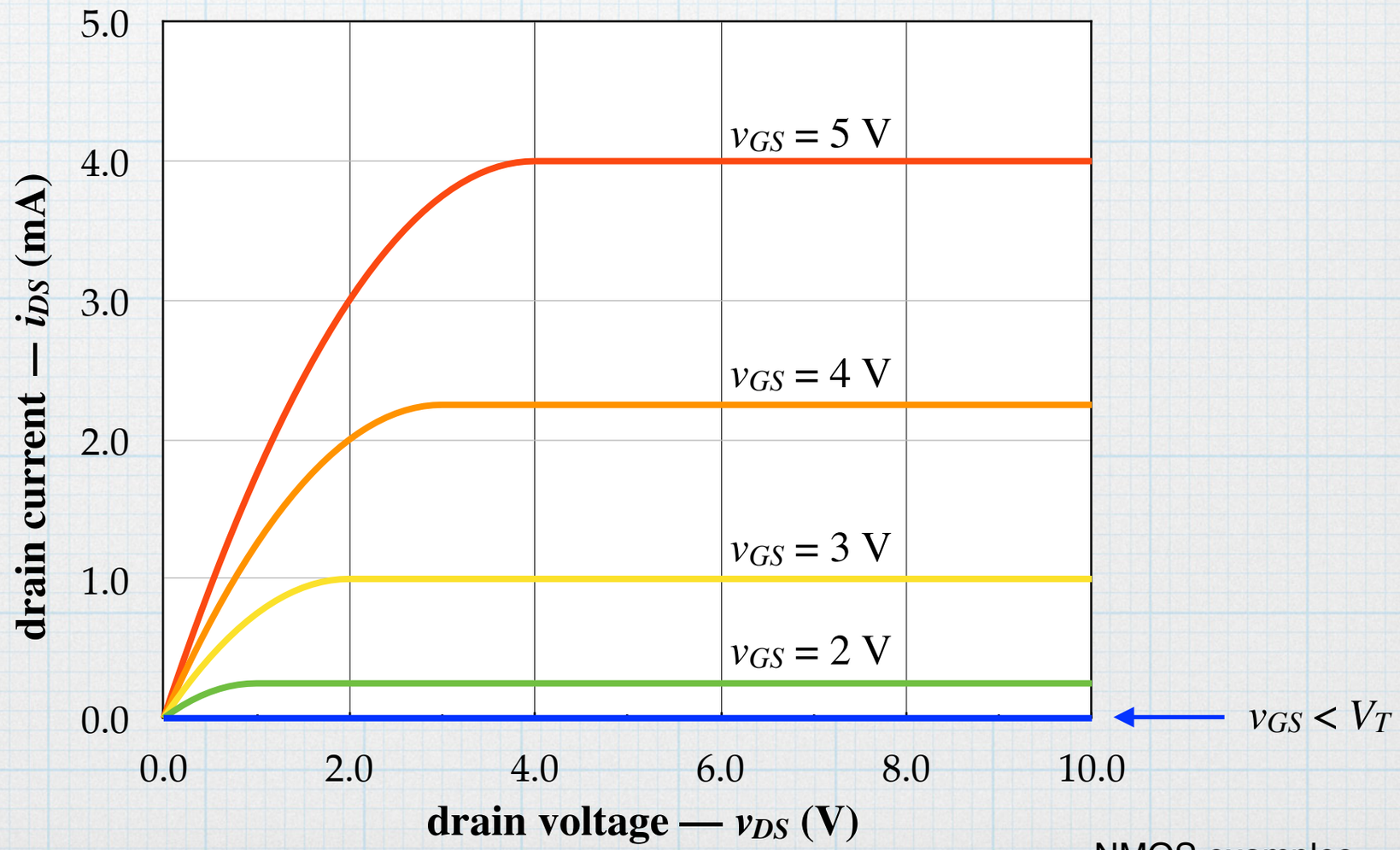
NMOS example problems

off	ohmic (linear)	saturation
$V_{GS} < V_T$	$v_{GS} \geq V_T$ $v_{DS} < v_{GS} - V_T$	$v_{GS} \geq V_T$ $v_{DS} \geq v_{GS} - V_T$
$i_D = 0$	$i_D = K_n \left[2 \left(v_{GS} - V_T \right) v_{DS} - v_{DS}^2 \right]$	$i_D = K_n \left[v_{GS} - V_T \right]^2$

$$K_n = \frac{1}{2} \mu_n C_{ox} \frac{W}{L}$$

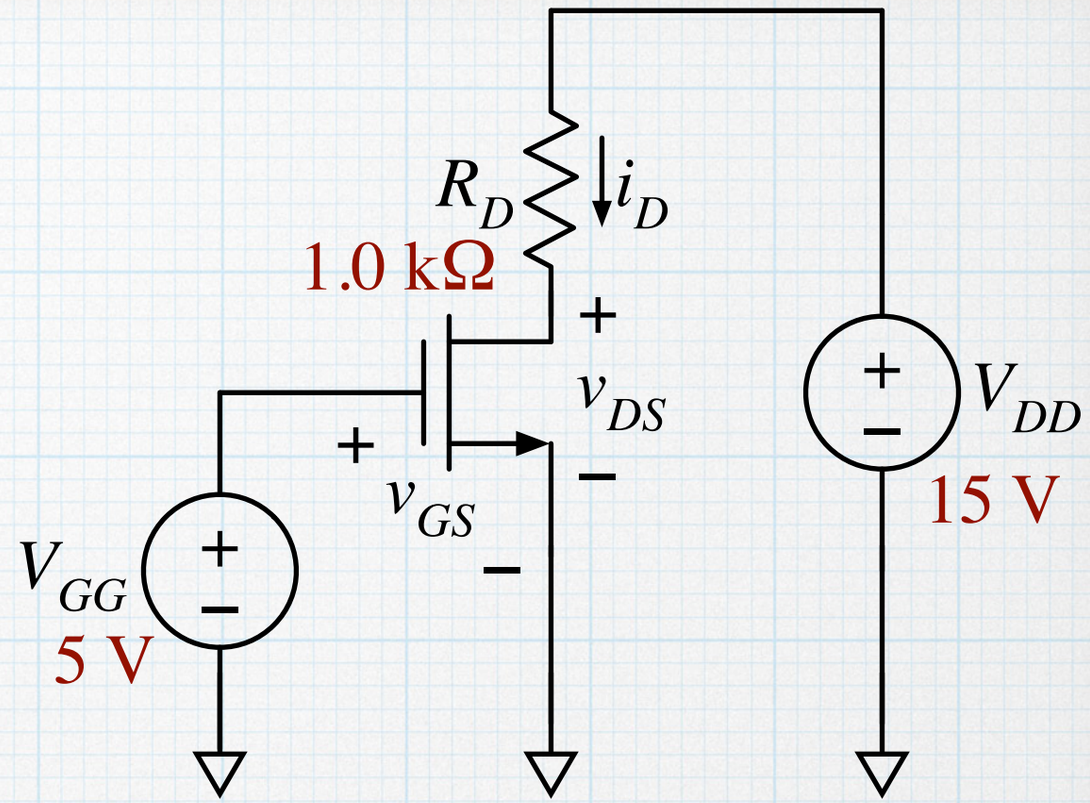
3-terminal symbol





Example 1

For the circuit shown, use the the NMOS equations to find i_D and v_{DS}.



For the NMOS, $V_T = 1\,\text{V}$ and $K_n = 0.5\,\text{mA/V}^2$.

We see that

$v_{GS} = V_{GG} = 5\,\text{V} > V_T \rightarrow$ the NMOS is on.

Guess that the transistor is in saturation.

$$i_D = K_n\left(v_{GS} - V_T\right)^2$$

$$= \left(0.5\,\text{mA/V}^2\right)\left(5\,\text{V} - 1\,\text{V}\right)^2 = 8\,\text{mA}$$

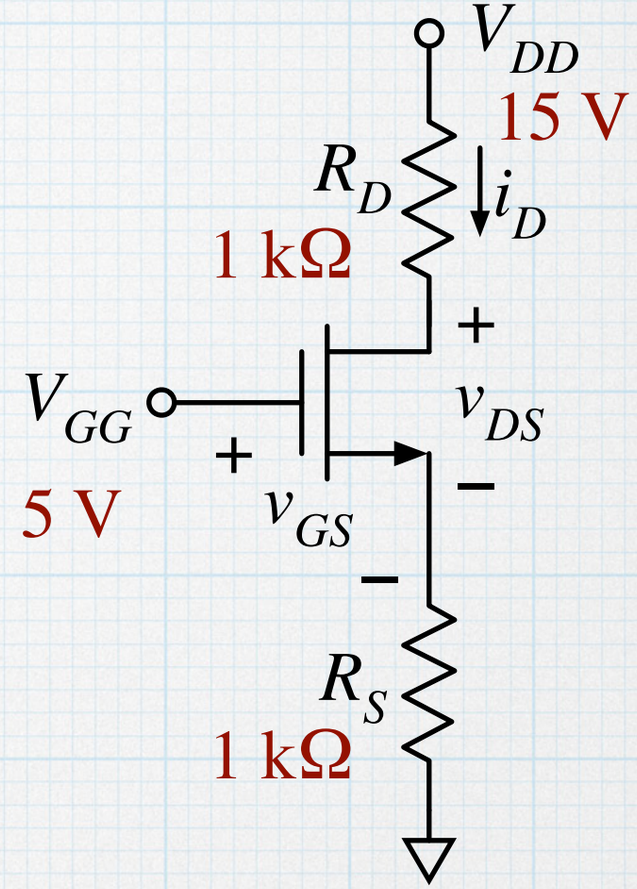
$$v_{DS} = V_{DD} - i_D R_D = 15\,\text{V} - \left(8.0\,\text{mA}\right)\left(1\,\text{k}\Omega\right) = 7\,\text{V}$$

$$v_{GS} - V_T = 4\,\text{V}$$

$v_{DS} > v_{GS} - V_T \rightarrow$ saturation confirmed. Q.E.D.

Example 2

For the circuit shown, use the the NMOS equations to find i_D and v_{DS}. (This looks a lot like Example 1, but the resistor connected to the source will change things.)



For the NMOS, $V_T = 1.0\,\text{V}$ and $K_n = 0.5\ \text{mA/V}^2$.

First, is the transistor on? The problem is that $v_{GS} = v_G - v_S$, and $v_S = i_D R_S$. Since we don't yet know i_D, we don't know the value of v_{GS}.

To help decide the issue, we could *guess* that the transistor is off, meaning that we are assuming $v_{GS} < V_T$. However, if the NMOS is off, then $i_D = 0$. This makes $v_{GS} = V_{GG} - i_D R_S = V_{GG} = 5\ \text{V}$. This is greater than V_T, meaning that the transistor should be on — in exact contradiction to the assumption of the transistor being off. So the transistor must be on.

Next, is the NMOS in saturation or ohmic? Here we can't even make a logical argument as we did in deciding on or off. So we must guess — let's guess saturation and see what happens.

Example 2 (cont.)

If the transistor is in saturation

$$i_D = K_n \left(v_{GS} - V_T\right)^2.$$

Also, we know that $v_{GS} = V_{GG} - i_D R_S$. Inserting into the saturation current equation:

$$i_D = K_n \left(V_{GG} - i_D R_S - V_T\right)^2$$

This is a quadratic equation for i_D. If we have the right type of calculator, we could type in this equation and hit "solve" to get the values (plural!) for i_D. Or we can limber up our algebra muscles and solve the old fashioned way. First expand the square: (Treat $V_{GG} - V_T$ as as single constant.)

$$i_D = K_n \left[\left(i_D R_S\right)^2 - 2\left(i_D R_S\right)\left(V_{GG} - V_T\right)^2 - \left(V_{GG} - V_T\right)^2\right]$$

Re-arranging and gathering terms:

$$i_D^2 - \left[2\left(\frac{V_{GG} - V_T}{R_S}\right) + \frac{1}{K_n R_S^2}\right] i_D + \left(\frac{V_{GG} - V_T}{R_S}\right)^2 = 0$$

Example 2 (cont.)

Now, using our old-fashioned calculator (Or slide rule. Or abacus. Or fingers and toes.), we can plug in the numbers.

$$i_D^2 - (10\,\text{mA})\,i_D + 16\,\text{mA}^2 = 0.$$

(Note the units on the third term.)

Use the quadratic formula to find

$$i_D = 2\ \text{mA or } i_D = 8\ \text{mA}.$$

So another conundrum: Which is it? Or both?

$$ax^2 + bx + c = 0$$

$$x = -\frac{b \pm \sqrt{b^2 - 4ac}}{2a}$$

If $a = 1$:

$$x = -\frac{b}{2} \pm \sqrt{\left(\frac{b}{2}\right)^2 - c}$$

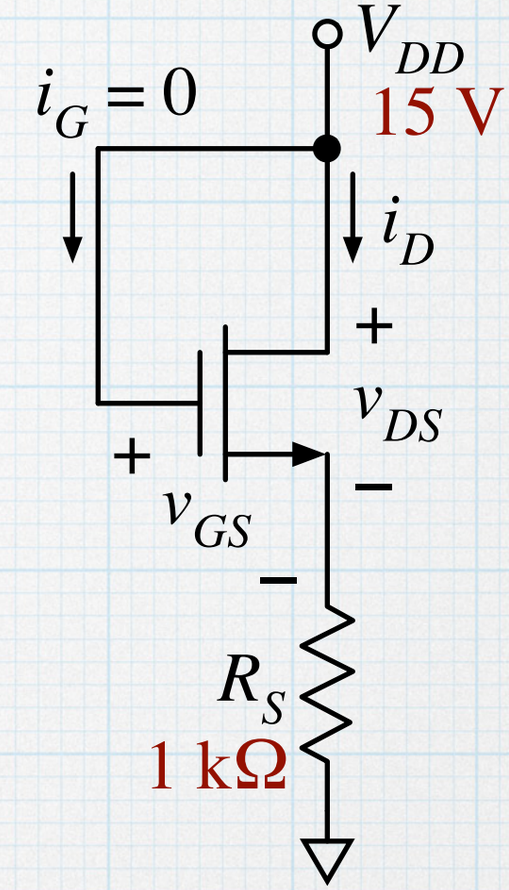
The correct solution must be consistent with the NMOS being on and in saturation. Only one root will meet both conditions. Start with $i_D = 8$ mA. In that case, $v_{GS} = V_{GG} - i_D R_S = 5\ \text{V} - (8\ \text{mA})(1\text{k}\Omega) = -3\ \text{V}$. This is (a lot) less than V_T. The larger root fails the "on" test rather badly.

Now consider $i_D = 2$ mA. In that case, $v_{GS} = 3\ \text{V} > V_T$. So the NMOS is clearly on. Next, $v_{DS} = V_{DD} - i_D R_D - i_D R_S = 15\ \text{V} - 2\ \text{V} - 2\ \text{V} = 11\ \text{V}$, which is clearly bigger than $v_{GS} - V_T = 2\ \text{V}$. The saturation assumption is also confirmed. So the correct answers are:

$$i_D = 2\ \text{mA and } v_{DS} = 11\ \text{V}.$$

Example 3

For the circuit shown, find i_D and v_{DS}. Calculate the power being dissipated in the NMOS and the resistor.



For the NMOS, $V_T = 1$ V and $K_n = 0.5$ mA/V^2.

We start by noting that the gate is tied to the drain — the NMOS is now essentially a term-terminal device. As always, there is no current flowing into the gate. Given the connections, is obvious that $v_{GS} = v_{DS}$. This means that the NMOS can either be off or in saturation. It cannot be in the ohmic mode of operation — with gate tied to drain, v_{DS} is *always* bigger than $v_{GS} - V_T$.

Then, by the same argument used in Example 2, we know that the NMOS must be on. If the NMOS must be on and it can't be in ohmic, then it must be operating in saturation:

$$i_D = K_n \left(v_{GS} - V_T\right)^2$$

and

$$v_{GS} = V_{DD} - i_D R_S.$$

Example 3 (cont.)

Putting the two equations together,

$$i_D = K_n \left(V_{DD} - i_D R_S - V_T \right)^2$$

We have almost the same situation as seen in example 2. We could plug the above into a calculator and solve. Or we can do a bit of algebra.

$$i_D = K_n \left[\left(i_D R_S \right)^2 - 2 \left(i_D R_S \right) \left(V_{DD} - V_T \right) - \left(V_{DD} - V_T \right)^2 \right]$$

Re-arranging and gathering terms:

$$i_D^2 - \left[2 \left(\frac{V_{DD} - V_T}{R_S} \right) + \frac{1}{K_n R_S^2} \right] i_D + \left(\frac{V_{DD} - V_T}{R_S} \right)^2 = 0.$$

Plugging in numbers:

$$i_D^2 - (30\,\text{mA})\, i_D + 196\,\text{mA}^2 = 0.$$

Using the quadratic equation to find the two roots:

$$i_D = 9.61\ \text{mA} \quad \text{or} \quad i_D = 20.39\ \text{mA}.$$

Example 3 (cont.)

We begin to recognize the pattern that will be common with MOSFETs — the solution will involve a quadratic equation with two possible roots. We must find the one root that is consistent with either what we already know or what we have assumed. In this case, the correct current must be consistent with the NMOS being on and in saturation.

If $i_D = 20.39$ mA, then,

$v_{GS} = V_{DD} - i_D R_S = 15\text{ V} - (20.39\text{ mA})(1\text{k}\Omega) = -5.39\text{ V}.$

If this were the case, the NMOS should be off. The NMOS cannot be both on and off at the same time, so this case fails the consistency test.

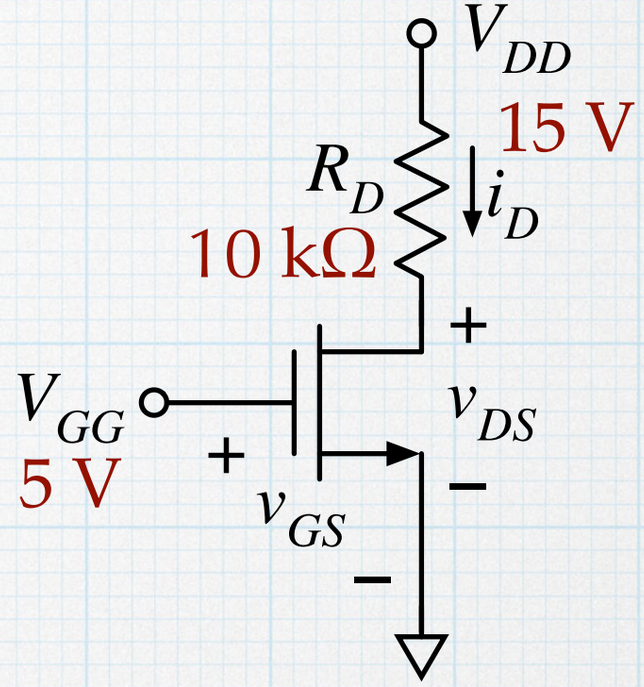
If $i_D = 9.61$ mA, then, $v_{GS} = 15\text{ V} - (9.61\text{ mA})(1\text{k}\Omega) = 5.39\text{ V}$. So the NMOS is clearly on. This the correct value for the current. And we know that the NMOS must be in saturation because $v_{DS} = v_{GS}$, so no need to check that. Finally:

$$P_{NMOS} = v_{DS} \cdot i_D = (5.39\text{ V})(9.61\text{ mA}) = 51.8\text{ mW}$$

$$P_{RS} = i_D^2 \cdot R_S = 92.4\text{ mW}.$$

Example 4

For the circuit shown, find i_D and v_{DS}.



For the NMOS, $V_T = 1\,\text{V}$ and $K_n = 0.5\,\text{mA/V}^2$.

This looks just like Example 1 — the only change change is in the value of R_D. this should easy.

As in Example 1

$$v_{GS} = V_{GG} = 5\,\text{V} > V_T \rightarrow \text{the NMOS is on.}$$

Assuming that the transistor is in saturation.

$$i_D = K_n\left(v_{GS} - V_T\right)^2$$

$$= \left(0.5\,\text{mA/V}^2\right)\left(5\,\text{V} - 1\,\text{V}\right)^2 = 8\,\text{mA}$$

$$v_{DS} = V_{DD} - i_D R_D = 15\,\text{V} - \left(8.0\,\text{mA}\right)\left(10\,\text{k}\Omega\right) = -65\,\text{V}$$

Whoa! Whoa! Whoa! There is a serious problem here. This value of v_{DS} is not consistent with being in saturation. Also, how could we possibly have –65 V when there are only positive power supplies?

Apparently the NMOS is **not** in saturation.

Example 4 (cont.)

The NMOS must be on, and if it is not in saturation, it must be operating in the ohmic (linear) mode. Using the ohmic equation:

$$i_D = K_n \left[2 \left(v_{GS} - V_T \right) v_{DS} - v_{DS}^2 \right]$$

We don't know either i_D or v_{DS}, so we will need a second equation. Fortunately, one is readily available. Write a node-voltage equation at the drain node.

$$i_D = \frac{V_{DD} - v_{DS}}{R_D}$$

Setting the two equal eliminates i_D and gives us a quadratic equation for v_{DS}.

$$\frac{V_{DD} - v_{DS}}{R_D} = K_n \left[2 \left(v_{GS} - V_T \right) v_{DS} - v_{DS}^2 \right]$$

We could plug into a calculator and solve. Or turn the algebra crank:

$$v_{DS}^2 - \left[2 \left(v_{GS} - V_T \right) + \frac{1}{K_n R_D} \right] + \frac{V_{DD}}{K_n R_D} = 0$$

Example 4 (con't)

Plugging in the values:

$$v_{DS}^2 - \left[8.2\,\text{V}\right] v_{DS} + 3\,\text{V}^2 = 0$$

(Again, note units on the third term.) Use the quadratic formula to find the roots:

$$v_{DS} = 0.384\ \text{V or } v_{DS} = 7.82\ \text{V}.$$

Once again, we must determine which of these is consistent with the transistor being in ohmic, meaning that the root should be less than $v_{GS} - V_T = 4$ V. The larger root is clearly too big. The smaller root works, so the correct answer is $v_{DS} = 0.384$ V. Then

$$i_D = \frac{V_{DD} - v_{DS}}{R_D} = \frac{15\,\text{V} - 0.384\,\text{V}}{10\,\text{k}\Omega} = 1.46\,\text{mA}$$

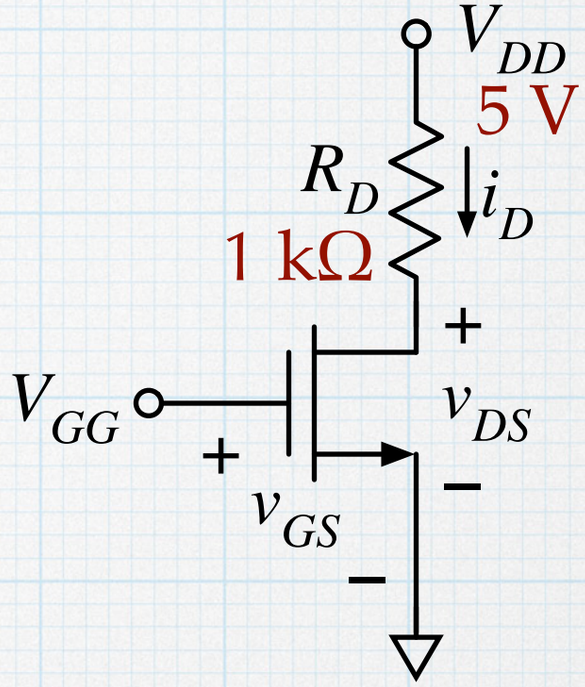
So the corrects answers are:

$$i_D = 1.46\ \text{mA and } v_{DS} = 0.384\ \text{V}.$$

Obviously, changing R_D had a big effect on the transistor's mode of operation.

Example 5

For the circuit shown, find i_D, v_{DS}, and calculate the power being dissipated in the NMOS and resistor for $V_{GG} = 0.5$ V, $V_{GG} = 2.5$ V, and $V_{GG} = 5$ V.



For the NMOS, $V_T = 1$ V and $K_n = 0.5$ mA/V^2.

Again, this looks very much like Example 1, with different applied voltages. Consider each in turn.

In all cases, $v_{DS} = V_{DD} - i_D R_D$. In each case, we must find either i_D or v_{DS}, and then other quantity is easily calculated.

$V_{GG} = 0.5$ V:

$v_{GS} = V_{GG} = 0.5$ V $< V_T$!! → the NMOS is off, and the current must be zero.

$$i_D = 0 \rightarrow v_{DS} = V_{DD} = 5 \text{ V}.$$

With $i_D = 0$, there is no power dissipated in either the transistor or the resistor.

Example 5 (cont.)

$V_{GG} = 2.5$ V:

Now, $v_{GS} = V_{GG} = 2.5\text{ V} > V_T$. →The NMOS is on.
Ohmic or saturation? It is not obvious, so let's guess saturation.

$$i_D = K_n\left(v_{GS} - V_T\right)^2$$

$$= \left(0.5\,\text{mA/V}^2\right)\left(2.5\,\text{V} - 1\,\text{V}\right)^2 = 1.125\,\text{mA}$$

Then

$$v_{DS} = V_{DD} - i_D R_D = 5\,\text{V} - \left(1.125\,\text{mA}\right)\left(1\,\text{k}\Omega\right) = 3.875\,\text{V}$$

Check:

$$v_{GS} - V_T = 1.5\,\text{V}$$

$v_{DS} > v_{GS} - V_T$ → saturation confirmed.

$P_{NMOS} = v_{DS} \cdot i_D = (3.875\text{ V})(1.125\text{ mA}) = 4.36\text{ mW}$

$P_{RS} = i_D{}^2 \cdot R_D = 1.27$ mW.

Example 5 (cont.)

$V_{GG} = 5$ V:

Now, $v_{GS} = V_{GG} = 5\text{ V} > V_T$ → the NMOS is still on.
Ohmic or saturation? We might suspect ohmic, but calculating saturation is easy, and there is not much penalty if we guess wrong.

$$i_D = K_n \left(v_{GS} - V_T\right)^2$$

$$= \left(0.5\,\text{mA/V}^2\right)\left(5\,\text{V} - 1\,\text{V}\right)^2 = 8\,\text{mA}$$

Then

$$v_{DS} = V_{DD} - i_D R_D = 5\,\text{V} - (8\,\text{mA})\left(1\,\text{k}\Omega\right) = -3\,\text{V}$$

Urk. Suspicion confirmed. It's not saturation so it must be ohmic. (See Example 4.)

$$i_D = K_n \left[2\left(v_{GS} - V_T\right) v_{DS} - v_{DS}^2\right]$$

Invoking a second equation:

$$v_{DS} = V_{DD} - i_D R_D$$

Example 5 (cont.)

We could do exactly as in Example 4, where we substituted for i_D and then solved the quadratic for v_{DS}. But to mix things up a bit, let's substitute for v_{DS}, resulting in a quadratic for i_D.

$$i_D = K_n\left[2\left(v_{GS}-V_T\right)\left(V_{DD}-i_D R_D\right)-\left(V_{DD}-i_D R_D\right)^2\right]$$

Use a calculator. Or precede with the algebra. Rearranging:

$$i_D^2+\left[\frac{2\left(v_{GS}-V_T\right)}{R_D}-\frac{2V_{DD}}{R_D}+\frac{1}{K_n R_D^2}\right]i_D+\left[\frac{V_{DD}^2-2\left(v_{GS}-V_T\right)V_{DD}}{R_D^2}\right]=0$$

(Hmm. This may have been easier the other way. Oh well.) Insert values.

$i_D^2 - 15\,\text{mA}^2 = 0$. (That's an interesting fluke of the numbers.)

The two roots are $i_D = -3.87$ mA or $i_D = +3.87$ mA. It is pretty easy to pick the plausible root — the negative value is impossible. So with $i_D = 3.87$ mA.

$v_{DS} = V_{DD} - i_D R_D = 1.13$ V

$P_{NMOS} = v_{DS} \cdot i_D = (1.13\text{ V})(3.87\text{ mA}) = 4.37$ mW

$P_{RS} = i_D{}^2 \cdot R_D = 15.0$ mW.

Example 6a

For the circuit shown, find i_D, v_{GS}, and v_{DS}.

For the NMOS, $V_T = 2\,\text{V}$ and $K_n = 0.25\,\text{mA/V}^2$.

(This is an old-timey way to set up the DC current in a transistor circuit.)

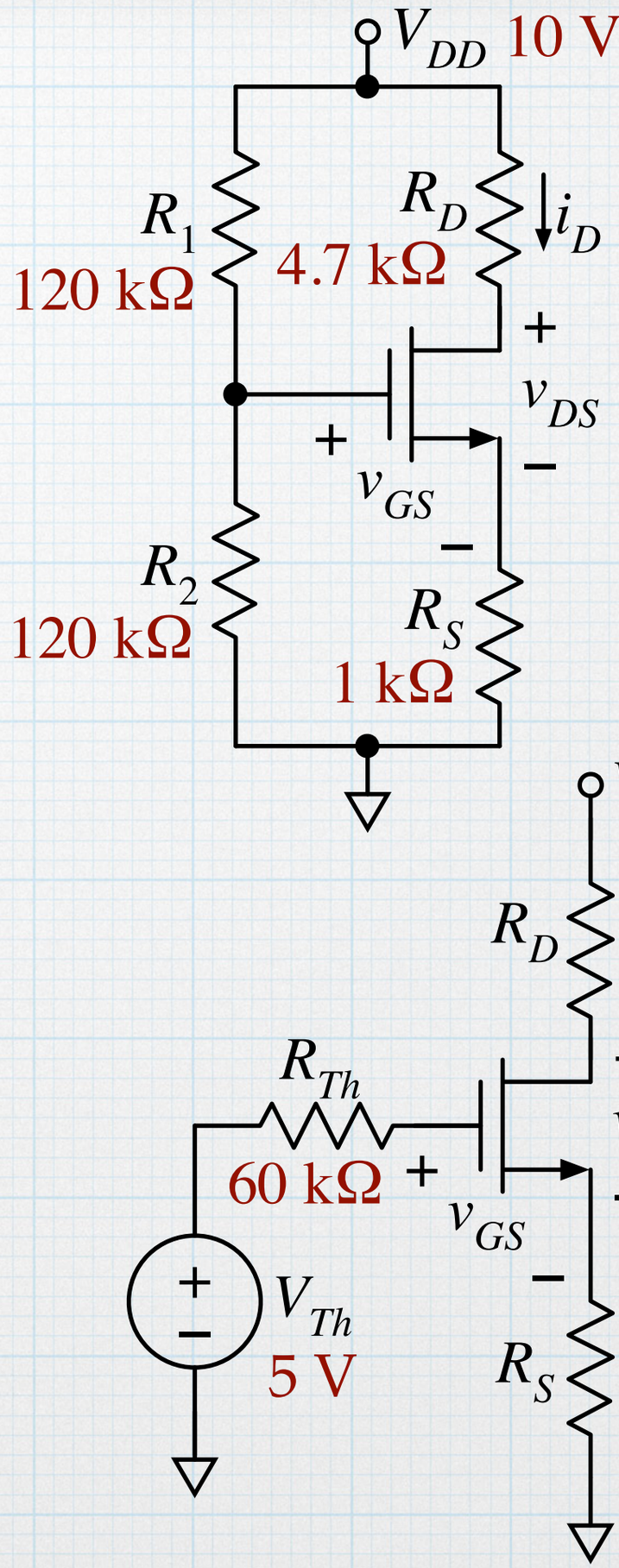
Start by finding the Thevenin equivalent between the gate and ground of R_1, R_2, and V_{DD}. (This is a classic from 201.)

$$V_{Th} = \frac{R_2}{R_1 + R_2} V_{DD} = 5\,\text{V}$$

and

$$R_{Th} = R_1 \| R_2 = 60\,\text{k}\Omega$$

However, R_{Th} is irrelevant since there is no DC gate current. Then the voltage at the gate is equal to V_{Th}, and the circuit is essentially identical to the one in Example 2.



Example 6a (cont.)

Since $V_{Th} > V_T$, the NMOS must on. Assuming it is in saturation:

$$i_D = K_n \left(v_{GS} - V_T\right)^2,$$

As seen in previous examples, $v_{GS} = V_{Th} - i_D R_S$. Inserting into the current equation gives the expected quadratic equation:

$$i_D = K_n \left(V_{Th} - i_D R_S - V_T\right)^2,$$

Solve it now with a calculator or do the algebra, which is nearly identical to previous examples. The end result is:

$$i_D^2 - \left[2\left(\frac{V_{Th} - V_T}{R_S}\right) + \frac{1}{K_n R_S^2}\right] i_D + \left(\frac{V_{Th} - V_T}{R_S}\right)^2 = 0$$

Plug in the numbers

$$i_D^2 - (10\,\text{mA})\, i_D + 9\,\text{mA}^2 = 0 \;\rightarrow\; i_D = 1\,\text{mA} \text{ or } i_D = 9\,\text{mA}$$

9 mA is too big, as we have seen before, so the correct value is 1 mA.

Then $v_{DS} = V_{DD} - i_D\left(R_D + R_S\right) = 4.3\,\text{V}$ and $v_{GS} = V_{Th} - i_D R_S = 4\,\text{V}$.

We see that $v_{DS} > v_{GS} - V_T$, consistent with the NMOS in saturation.

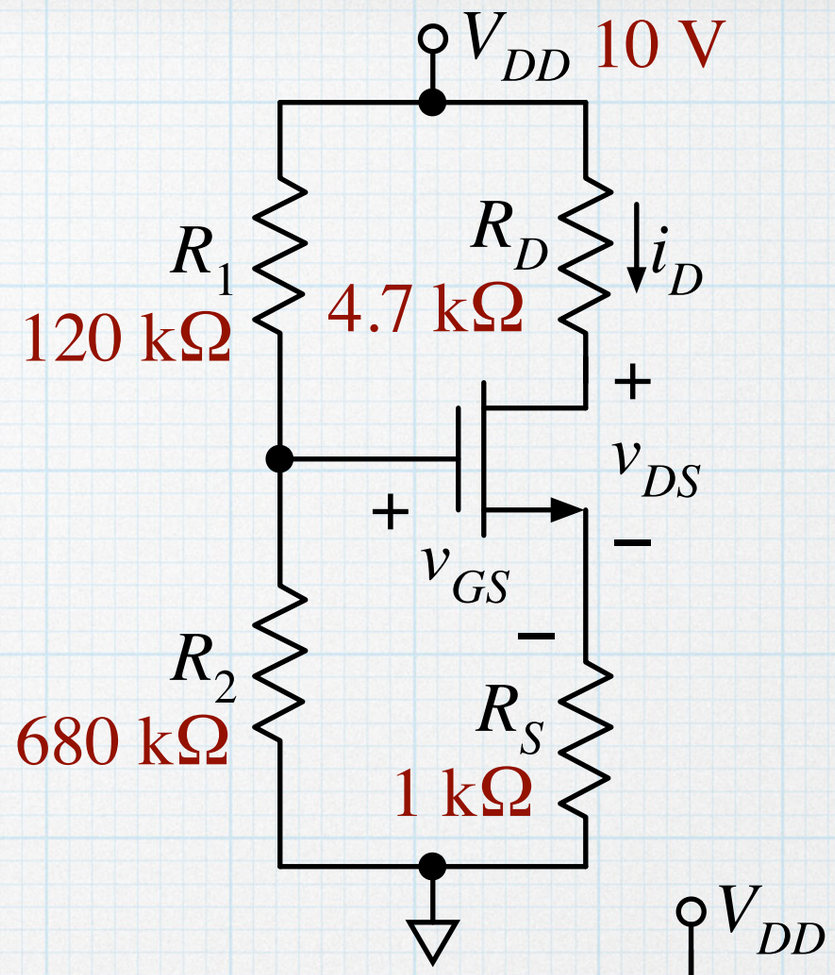
Example 6b

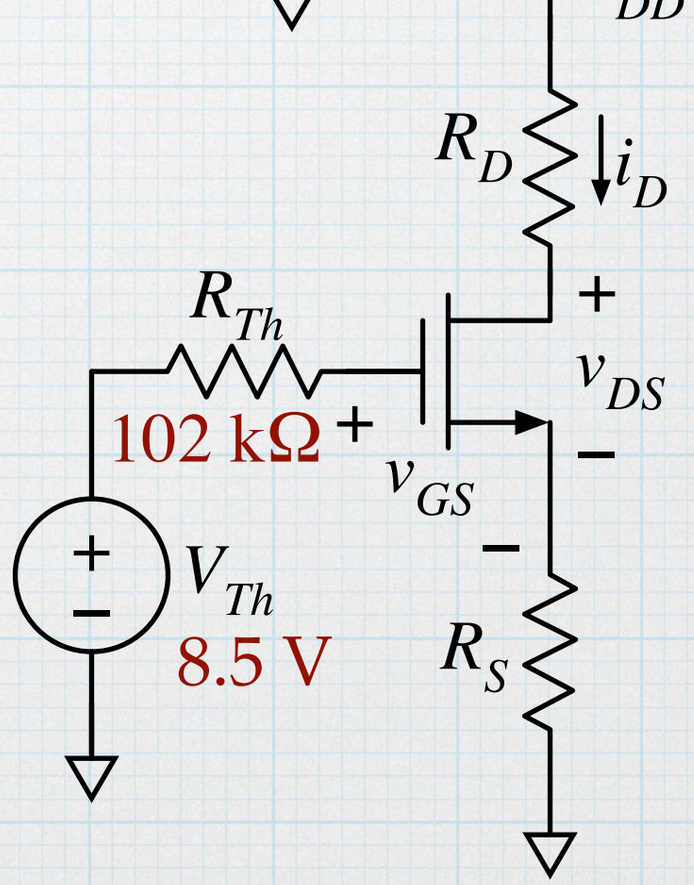
Same as example 6a, but the value for R_2 is increased to 680 kΩ. It is the same NMOS: $V_T = 2$ V and $K = 0.25$ mA/V².

Following the same procedure as Example 6a, we use the Thevenin between the gate and ground: $V_{Th} = 8.5$ V and $R_{Th} = 102$ kΩ. (R_{Th} is still irrelevant.)

We have seen enough examples already that we might be a bit suspicious about this one. The larger voltage at the gate implies that there will be more drain current, and the larger current will lead to a smaller v_{DS}. The NMOS may well be working in the ohmic mode. So let's start by guessing ohmic, in which case the current is

$$i_D = k_n \left[2 \left(v_{GS} - V_T \right) v_{DS} - v_{DS}^2 \right].$$





Example 6b (cont.)

In the ohmic current equation, we don't know i_D, v_{GS}, or v_{DS}. So we need more equations. For v_{GS} and v_{DS}, we can write:

$$v_{GS} = V_{Th} - i_D R_S \quad \text{and} \quad v_{DS} = V_{DD} - i_D R_D - i_D R_S.$$

Plugging in:

$$i_D = K_n \left[2 \left(V_{Th} - i_D R_S - V_T \right) \left(V_{DD} - i_D R_D - i_D R_S \right) - \left(V_{DD} - i_D R_D - i_D R_S \right)^2 \right].$$

Yikes! This looks very unpleasant. Plug into a solver. Or do the algebra (Urk):

$$i_D^2 + \left[\frac{2 \left(V_{Th} - V_T \right) \left(R_S + R_D \right) - 2 V_{DD} R_D + \frac{1}{K_n}}{R_S^2 - R_D^2} \right] i_D + \left[\frac{2 \left(V_{Th} - V_T \right) V_{DD} - V_{DD}^2}{R_S^2 - R_D^2} \right] = 0$$

(Note that we must be careful if $R_S = R_D$. But, if they are equal, it is no longer a quadratic — the math is actually a bit easier.) Now plug in numbers:

$$i_D^2 - \left(0.7539\,\text{mA} \right) i_D - 1.4225\,\text{mA}^2 = 0 \;\rightarrow\; i_D = 1.63\,\text{mA} \text{ or } i_D = -0.874\,\text{mA}$$

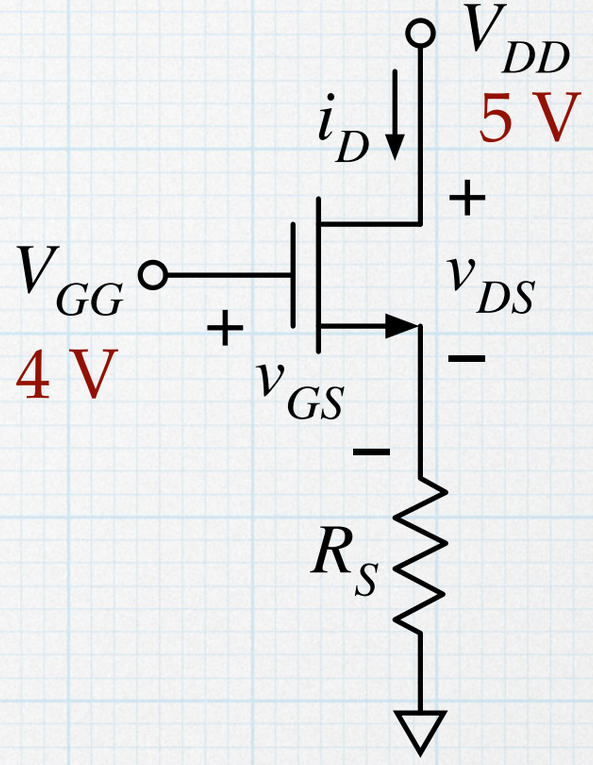
The negative value is not possible, so the correct current is 1.63 mA.

Then $v_{DS} = V_{DD} - i_D \left(R_D + R_S \right) = 0.721\,\text{V}$ and $v_{GS} = V_{Th} - i_D R_S = 6.87\,\text{V}$.

We see that $v_{DS} < v_{GS} - V_T$, consistent with the NMOS in ohmic. Whew!

Example 7

Design the circuit at right (by choosing K_n for the NMOS and the value of R_S) so that $i_D = 1$ mA and $v_{DS} = 2.5$ V. The NMOS has $V_T = 1$ V.



By writing a loop equation around the drain-source loop, we see that $v_{RS} = V_{DD} - v_{DS} = 2.5$ V. And so the value of should be

$$R_S = (2.5\text{ V})/(1\text{ mA}) = 2.5\text{ k}\Omega.$$

Now writing a loop equation around the gate-source loop, we see that

$$v_{GS} = V_{GG} - v_{RS} = 4\text{ V} - 2.5\text{ V} = 1.5\text{ V}.$$

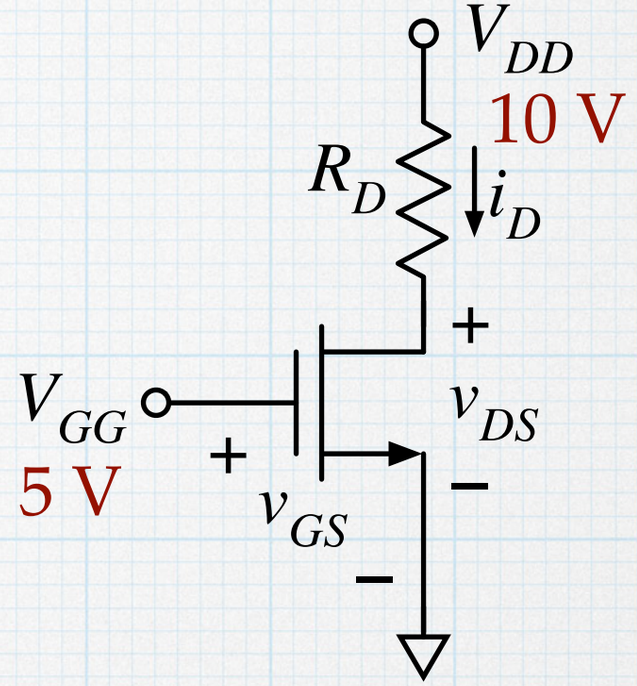
Since $v_{DS} = 2.5$ V, having $v_{GS} = 1.5$ V means that the NMOS will be operating in saturation.

In saturation, $i_D = K_n\left(v_{GS} - V_T\right)^2$, so

$$K_n = \frac{i_D}{\left(v_{GS} - V_T\right)^2} = \frac{1\text{ mA}}{\left(1.5\text{ V} - 1.5\text{ V}\right)^2} = 4\frac{\text{mA}}{\text{V}^2}$$

Example 8

Design the circuit at right (by choosing K_n for the NMOS and the value of R_D) so that $i_D = 10$ mA and $v_{DS} = 0.2$ V. The NMOS has $V_T = 1$ V. How much power is being dissipated in the resistor and the NMOS?



Using KVL, if $v_{DS} = 0.2$ V, then $v_{RD} = 9.8$ V.

For a current of 10 mA,

$R_D = v_{RD} / i_D = (9.8\text{ V})/(10\text{mA}) = 0.98\text{ k}\Omega$.

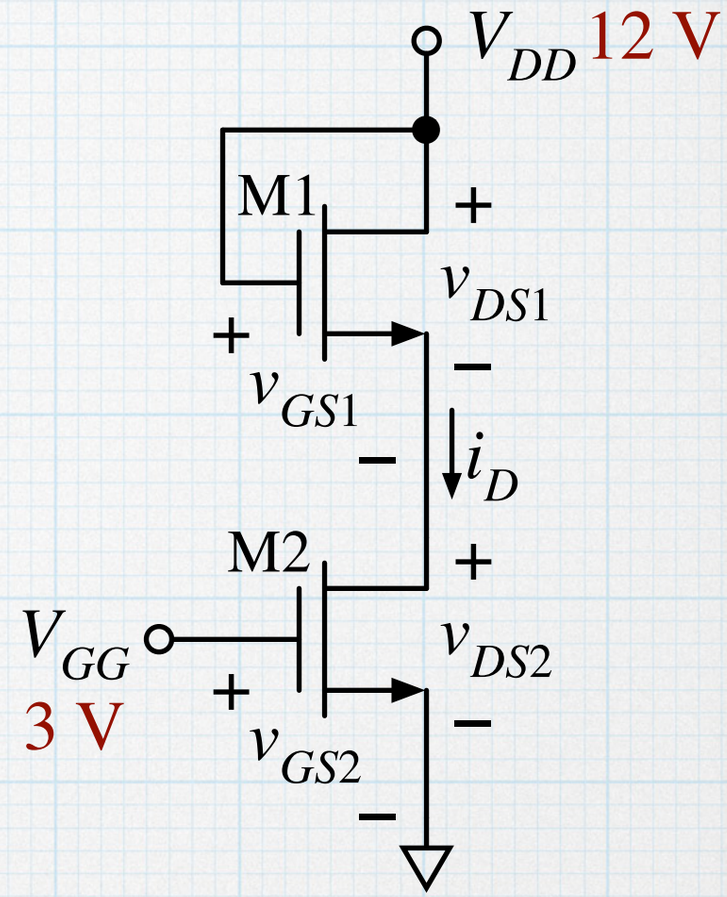
We see that $v_{GS} = V_{GG} = 5$ V and with $v_{DS} = 0.2$ V, the NMOS must be working in the ohmic region. For ohmic operation, $i_D = K_n \left[2\left(v_{GS} - V_T\right) v_{DS} - v_{DS}^2\right]$.

$$K_n = \frac{i_D}{2\left(v_{GS} - V_T\right) v_{DS} - v_{DS}^2} = \frac{10\,\text{mA}}{2\left(5\,\text{V} - 1\,\text{V}\right)(0.2\,\text{V}) - (0.2\,\text{V})^2} = 6.41\,\frac{\text{mA}}{\text{V}^2}$$

$$P_{RD} = (10\,\text{mA})(9.8\,\text{V}) = 98\,\text{mW} \qquad P_{NMOS} = (10\,\text{mA})(0.2\,\text{V}) = 2\,\text{mW}$$

Example 9

For the circuit shown, find i_D, v_{DS1}, and v_{DS2} for the two NMOS transistors in the circuit at right. Also, calculate the power being dissipated in each.



The two NMOS transistors have the same $V_T = 1$ V, the same $\mu_n C_{ox} = 0.1$ mA/V^2, and the same gate length, $L = 0.1\ \mu$m. The gate width for M1 is $W_1 = 0.2\ \mu$m, and for M2 $W_2 = 0.8\ \mu$m.

$$K_{n1} = \frac{1}{2}\mu_n C_{ox}\frac{W_1}{L} = 0.1\frac{\text{mA}}{\text{V}^2} \quad \text{and} \quad K_{n2} = 0.4\frac{\text{mA}}{\text{V}^2}.$$

Two NMOSs in one circuit! No resistors! Panic! Actually, no need to panic — the basic rules still apply. Start by recalling that there are no gate currents to consider, so $i_{D1} = i_{D2}$. (We will just call it i_D.)

Next, we note that the M1 is connected gate to drain — it must be operating in saturation.

Also, using KVL, we know that $V_{DD} = v_{DS1} + v_{DS2}$.

Finally, $v_{GS2} = V_{GG}$, and it is big enough to ensure that M2 is on. We can then guess either saturation or ohmic operation. We will guess saturation.

Example 9 (cont.)

If M2 is in saturation, then

$$i_D = K_{n2}\left(V_{GG} - V_T\right)^2 = \left(0.4\,\frac{\text{mA}}{\text{V}^2}\right)\left(3\,\text{V} - 1\,\text{V}\right)^2 = 1.6\,\text{mA}$$

The same current flows in M1, which we know must be in saturation. With $v_{GS1} = v_{DS1}$, we can write

$$i_D = K_{n1}\left(v_{GS1} - V_T\right)^2 = K_{n1}\left(v_{DS1} - V_T\right)^2$$

$$v_{DS1} = V_T \pm \sqrt{\frac{i_D}{K_{n1}}} = 1\,\text{V} \pm \sqrt{\frac{1.6\,\text{mA}}{0.1\,\frac{\text{mA}}{\text{V}^2}}} = 1\,\text{V} \pm 4\,\text{V}$$

The drain-to-source voltage for M1 cannot be negative, so $v_{DS1} = 5$ V.

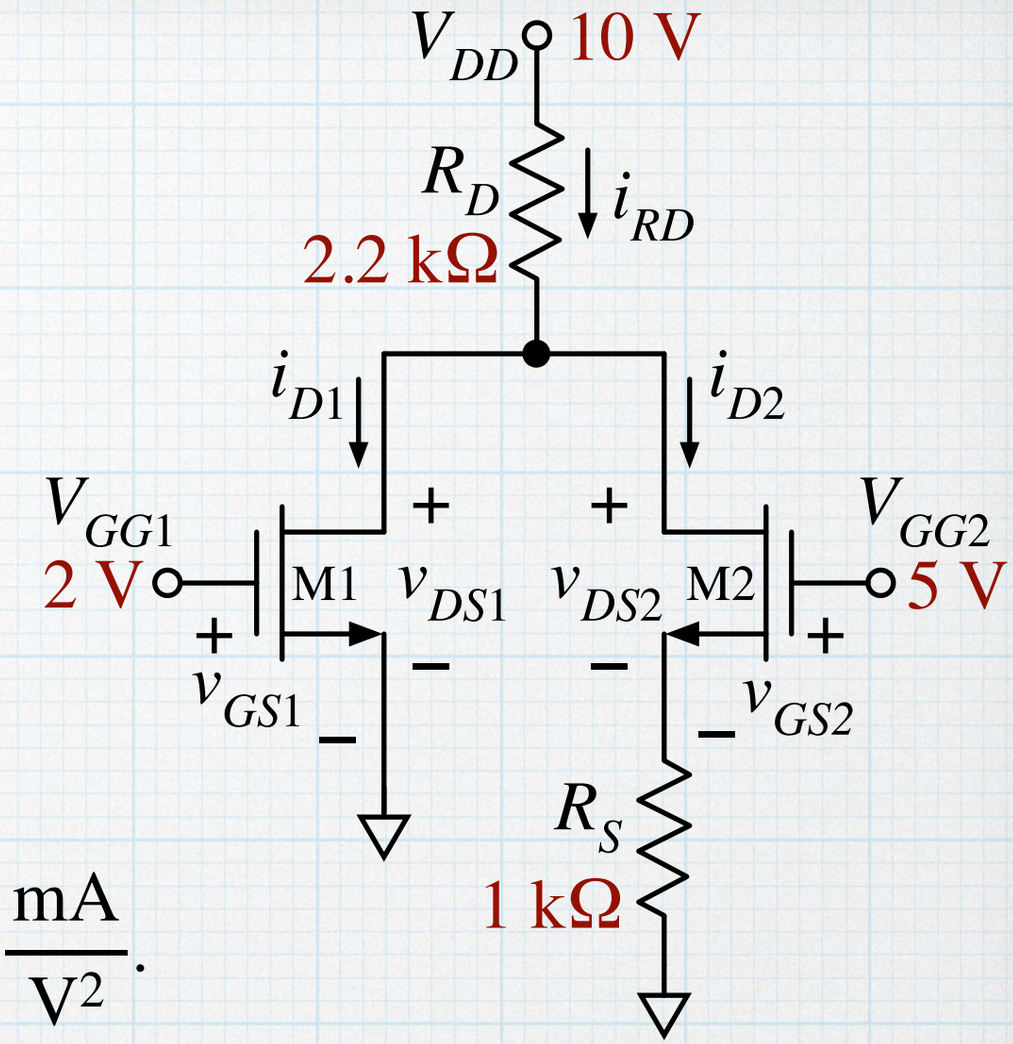
Finally, $v_{DS2} = V_{DD} - v_{DS1} = 7$ V.

Checking M2: v_{DS2} is greater than $v_{GS2} - V_T$, so saturation mode is confirmed.

Finally, $P_{M1} = v_{DS1} i_D = 8\,\text{mW}$ and $P_{M2} = v_{DS2} i_D = 11.2\,\text{mW}$.

Example 10

For the circuit shown, find i_{D1}, v_{DS1}, i_{D2}, and v_{DS2} for the two NMOS transistors at right.



The two NMOS transistors have the same $V_T = 1$ V, the same $\mu_n C_{ox} = 0.1$ mA/V^2, and the same gate length, $L = 1\ \mu$m. The gate width for M1 is 10 μm, and the gate width for M2 is 5 μm.

$$K_{n1} = \frac{1}{2}\mu_n C_{ox}\frac{W_1}{L} = 0.5\frac{\text{mA}}{\text{V}^2} \quad \text{and} \quad K_{n2} = 0.25\frac{\text{mA}}{\text{V}^2}.$$

Again, no need to panic. Let's start with a KCL equation: $i_{D1} + i_{D2} = i_{RD}$

Then we note that $v_{GS1} = V_{GG1}$ and $v_{GS2} = V_{GG2} - i_{D2}R_S$. Since both V_{GG1} and V_{GG2} are greater than V_T, both transistors will be on. (Refer back to earlier examples to see those arguments again.)

Now, we have to guess for each NMOS: ohmic or saturation?

Let's try saturation for both. In that case, i_{D1} is easy

$$i_{D1} = K_{n1}\left(V_{GG1} - V_T\right)^2 = 0.5\,\text{mA}.$$

Example 10 (cont.)

And for M2 in saturation:

$$i_{D2} = K_{n2}\left(v_{GS2} - V_T\right)^2 = K_{n2}\left(v_{GG2} - i_{D2}R_S - V_T\right)^2$$

We have solved that one before (see Example 2), either directly with a calculator or with some familiar algebra:

$$i_D^2 - \left[2\left(\frac{V_{GG2} - V_T}{R_S}\right) + \frac{1}{K_{n2}R_S^2}\right] i_D + \left(\frac{V_{GG2} - V_T}{R_S}\right)^2 = 0$$

$$i_D^2 - (12\,\text{mA})\, i_D + 16\,\text{mA}^2 = 0 \;\rightarrow\; i_{D2} = 1.53\,\text{mA} \text{ or } i_{D2} = 7.47\,\text{mA}$$

As we've seen before, the larger value is not consistent with M2 being in saturation, so $i_{D2} = 1.53$ mA, and $v_{GS2} = V_{GG2} - i_{D2}R_S = 3.47\,\text{V}$.

We must be careful with calculating the drain-source voltages — the current through R_D is $i_{D1} + i_{D2} = 2.03$ mA. So, the voltage across R_D is then 4.46 V.

$$v_{DS1} = V_{DD} - v_{RD} = 5.54\,\text{V} \text{ and } v_{DS2} = V_{DD} - v_{RD} - i_{D2}R_S = 4.01\,\text{V}.$$

Both values are consistent with the transistors being in saturation. This wasn't too hard. (Although if one or both transistors were operating in ohmic… 🤯)