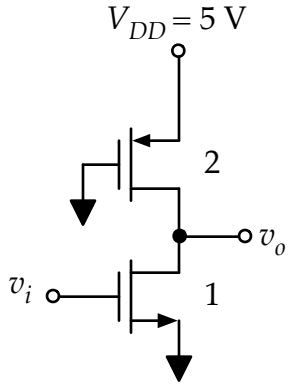
EE 230 — HW 6.9 Name_____

The circuit at right is known as a "pseudo-NMOS" inverter. (Note that is very similar to CMOS except that the PMOS gate voltage is fixed at $-V_{DD}$.)



In the circuit, the NMOS has $V_{TN} = 1$ V and $K_N = 0.5$ mA/V^2.
The PMOS has $V_{TP} = -1$ V and $K_P = 0.1$ mA/V^2.

Calculate the output voltage and total power being dissipated in the circuit for $v_i = 0.5$ V, 2.5 V, and 5 V.

$v_i = 0.5$ V: $v_o =$ _____, $P_{inv} =$ _____

$v_i = 2.5$ V: $v_o =$ _____, $P_{inv} =$ _____

$v_i = 5.0$ V: $v_o =$ _____, $P_{inv} =$ _____

Finally, use SPICE to make a plot of the voltage transfer characteristic. In PSPICE, use the MbreakN and MbreakP models with appropriate values for K_n and K_p.