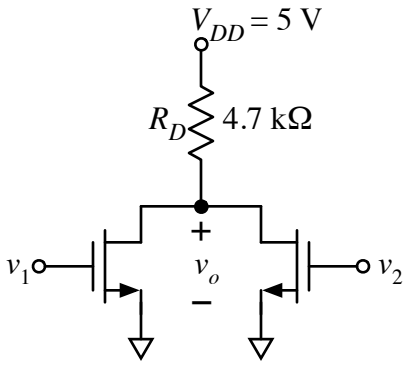
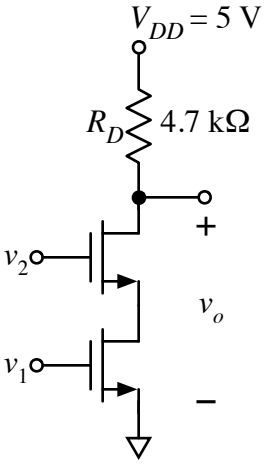
EE 230 — HW 6.5 Name_____

a. For the circuit at right, the input voltages, v_1 and v_2, can be either 0 V or 5 V. Calculate v_o for all four possible combinations of v_1 and v_2. The two NMOS transistors are identical with $V_{Tn} = 1$ V and $K_n = 0.1$ mA/V^2. (Don't panic. Make a reasonable guess for NMOS modes — off, sat, or ohmic — and check. Patterns will quickly become evident.) None of these cases are hard, but the one slightly more difficult case can simplified by assuming that two transistors working in parallel could be viewed as a single "bigger" transistor.



v_1	0 V	5 V	0 V	5 V
v_2	0 V	0 V	5 V	5 V
v_o				

b. For the circuit at right, the input voltages, v_1 and v_2, can be either 0 V or 5 V. Calculate v_o for all four possible combinations of v_1 and v_2. Same NMOS transistors as part a. Three cases are trivial, and the fourth is extremely difficult to do exactly using the ohmic equations. It can be done, but the amount of work is not worth the result. Instead, here three three proposed methods to come up with an answer. Pick one and see if you can work it out. The first two are analytical short cuts (and hence approximations). The third is SPICE.



1. When $v_1 = v_2 = 5$ V, both NMOSs should be in ohmic. In ohmic, if v_{DS} is sufficiently small, we can neglect the v_{DS}^2 term from the ohmic equation. That should make the math simpler. See if you can work it out with that approximation.

2. In ohmic, the NMOS is essentially a resistor. Calculate the effective drain resistance of the NMOSs for $v_{GS} = 4$ V. (That's not quite right for NMOS 2, but we will go with it.) Since the 2 FETs are now essentially resistors, we can use a voltage divider to find v_o. (EE 201 to the rescue.)

3. Work through the MOS SPICE notes, and then use your new-found knowledge to solve this with SPICE.

v_1	0 V	5 V	0 V	5 V
v_2	0 V	0 V	5 V	5 V
v_o				

Put your answers — and whatever work will fit — on this sheet. Staple any sheets with additional work behind.